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# Ultrahigh-Performance Inverters Based on CdS Nanobelts

**Peicai Wu, Yu Ye, Tuo Sun, Ruoming Peng, Xiaonan Wen, Wanjin Xu, Cui Liu, and Lun Dai***

State Key Lab for Mesoscopic Physics and Department of Physics, Peking University, Beijing 100871, China

**ABSTRACT** We report ultrahigh-performance inverters, each consisting of two top-gate metal−oxide−semiconductor field-effect transistors based on *n*-CdS nanobelts. High-κ $HfO_2$ dielectrics are used as the top-gate oxide layers. The inverters have a large supply voltage ($V_{DD}$) range (from 50 mV to 10 V) and very high voltage gain (~10, 100, and 1000 at $V_{DD}$ = 0.2, 1, and 10 V, respectively). Current consumption is less than 7 nA at $V_{DD}$ = 1 V, corresponding to a power consumption of less than 7 nW. The high and low output voltages are close to full rail. The inverters also exhibit good dynamic behavior with square wave input at frequencies up to 1 kHz. The operation of the inverters is analyzed in detail. The inverters are promising for future low power high performance logic circuit applications.

**KEYWORDS:** CdS · high-κ dielectrics · nanobelt · field-effect transistors · inverter

Semiconductor nanomaterials have shown their unique virtues as the building material for powerful electronic devices. Inverters are important building blocks in the integrated circuits. They can be constructed with field-effect transistors (FETs) of various materials. In the area of nanoelectronics, various types of inverters, such as resistor-load,[1,2] *p* -channel metal-oxide-semiconductor (PMOS),[3−6] *n*-channel MOS ( NMOS), [7,8] complementary MOS (CMOS), [9−15] *n*-channel metal−semiconductor (NMES),[16] and complementary MES (CMES)[17] inverters have been developed based on various nanomaterials, such as thin films, nanowires/nanobelts (NWs/NBs), carbon nanotubes (CNTs), and graphene. So far, most reported inverters based on semiconductor nanomaterials work under supply voltages ($V_{DD}$) larger than 0.4 V and have voltage gain less than 100. Power consumption is an increasingly important issue in general purpose processors. As transistors become smaller and faster, static power dissipation will increase significantly. Complementary inverters having both *n*- and *p*-channel transistors have a key inherent characteristic of low static power consumption. However, many important semiconductor nanoelectronic materials, such as CdS, CdSe, and $Zn_3P_2$ *etc.*, are unipolar materials.[16−20] In other words, they tend to exhibit only one conductivity type due to the strong self-compensation effect. This will limit their application in constructing high-performance complementary inverters. Exploring NMOS and/or PMOS inverters with improved performance characteristics, such as voltage gain, supply voltage, and power consumption, is still urgent in the practical application of nanomaterial circuits.

In this paper, we report NMOS inverters constructed with two top-gate MOSFETs based on *n*-CdS NBs. The two MOSFETs have different threshold voltages ($V_{th}$). The inverters can work under supply voltages down to 50 mV at room temperature and have a voltage gain of up to ~1000 at the $V_{DD}$ of 10 V. These characteristics, as far as we know, are the best

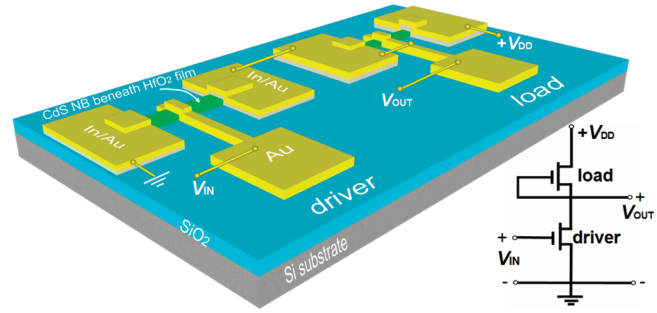


**Figure 1. Schematic illustration of an as-fabricated inverter. The golden lines show the way the circuit is connected. The inset is the corresponding circuit diagram.**

*Address correspondence to lundai@pku.edu.cn.

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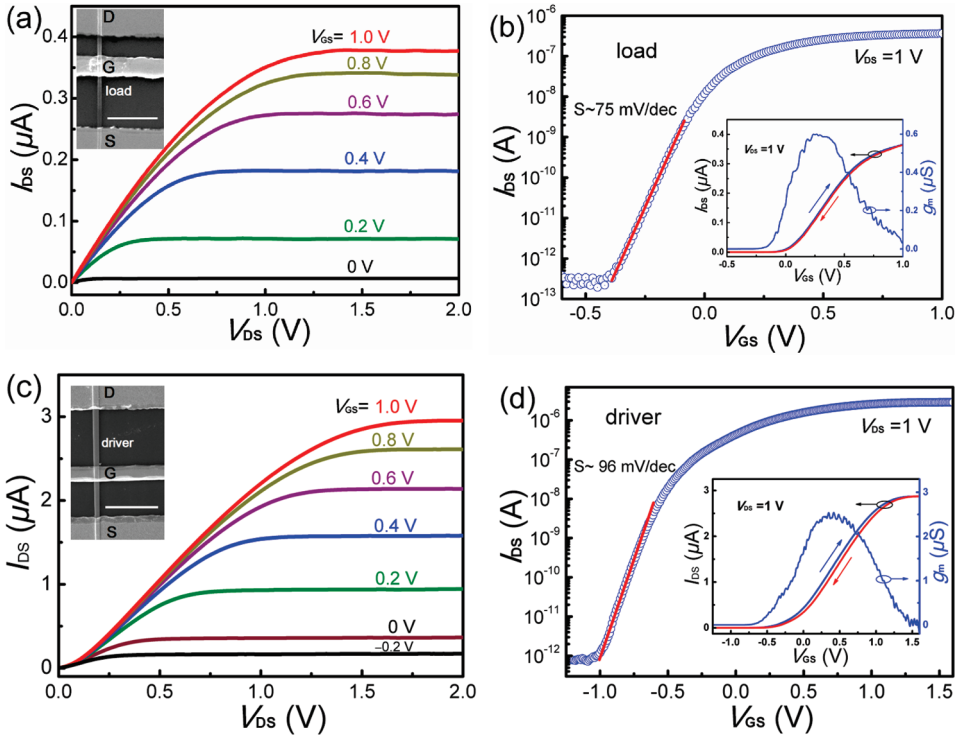


**Figure 2. (a) A family of $I_{DS}$ *versus* $V_{DS}$ curves measured at different $V_{GS}$ of the load MOSFET. The inset shows the FESEM image of the device (scale bar: 10 μm). (b) Gate transfer characteristic of the load at $V_{DS}$ = 1 V. The straight red line highlights the subthreshold region. The inset shows the $I_{DS}-V_{GS}$ hysteresis and transconductance curves. The curves in same color are measured simultaneously. (c) A family of $I_{DS}$ *versus* $V_{DS}$ curves measured at different $V_{GS}$ of the driver MOSFET. The inset shows the FESEM image of the device (scale bar: 10 μm). (d) Gate transfer characteristic of the driver at $V_{DS}$ = 1 V.**

among the inverters based on nanomaterials reported so far. The current ($I_{DD}$) flowing through the inverter ($V_{DD}$ = 1 V) is less than 7 nA, corresponding to a power consumption of less than 7 nW, which is so far the lowest reported value for NMOS and/or PMOS inverters. The operation of the inverters is analyzed in detail. The dynamic characteristics of the inverters are also studied. The inverters show good dynamic behaviors with output rising and falling times of about 0.25 and 0.03 ms, respectively, at square wave input frequency up to 1 kHz.

## RESULTS AND DISCUSSION

Figure 1 shows the schematic illustration of an as-fabricated inverter. The golden lines show the way the circuit is connected. The inset is the corresponding circuit diagram. Static electrical trans-port measurements were done with a semiconductor characterization system (Keithley 4200). Dynamic behaviors of the inverters were investigated with a digital oscilloscope (Tektronix DPO 2024) and square waves. All the measurements were done in darkness at room-temperature.

Figure 2a shows a family of source-drain current ($I_{DS}$) *versus* source-drain voltage ($V_{DS}$) curves measured at different gate voltages ($V_{GS}$) of the load MOSFET. The inset is a field-emission scanning electron microscope (FESEM) image of this transistor. The NB used (NB A) is about 0.86 μm wide and 133 nm thick. Figure 2b is the gate transfer characteristics at $V_{DS}$ = 1 V. An on/off ratio of about 6 × $10^6$ is obtained. The threshold voltage $V_{th}$ is very low (−0.1 V), which is beneficial to the low power inverter described below. The $I_{DS}-V_{GS}$ relation in the subthreshold region (the straight red line) gives a subthreshold swing $S$ of ~75 mV/dec. The inset shows the $I_{DS}-V_{GS}$ hysteresis and transconductance ($g_m$) curves, which exhibit a very small hysteresis and a peak $g_m$ value of about 0.6 μS, respectively. The field-effect electron mobility ($\mu_e$) of this MOSFET can be estimated to be about 18.6 $cm^2/V \cdot s$ using the equation $\mu_e = L_C g_m/(WC_0V_{DS})$,[21] where $L_C$ is the channel length (20 μm), $C_0$ is the oxide capacitance per unit area ($= \varepsilon_r\varepsilon_0/d$), $\varepsilon_r$ is the relative dielectrics constant of $HfO_2$ (~17), $W$ is the gate width (equal to the width of NB in the FET) and $d$ is the thickness (20 nm) of the $HfO_2$ layer. Decrease of mobility is commonly observed in MOSFETs with high-κ dielectrics, which is attributed to the carrier scattering caused by interface states between the high-κ dielectrics and the semiconductor conductive channel.[18,21,22] Figures 2c and 2d show the transfer characteristics of the driver MOSFET. The NB used (NB B) is about 1.1 μm wide and 125 nm thick. This MOSFET has a $V_{th}$ of about −0.65 V, an on/off ratio of about 2 × $10^6$, a subthreshold swing of about 96 mV/dec, and a peak $g_m$ value of about 2.5 μS. The field-effect electron mobility of this MOSFET can be estimated to be about 60.5 $cm^2/V \cdot s$ using the above-mentioned equation. Figure 3a is the static voltage transfer characteristic (VTC) curves of the

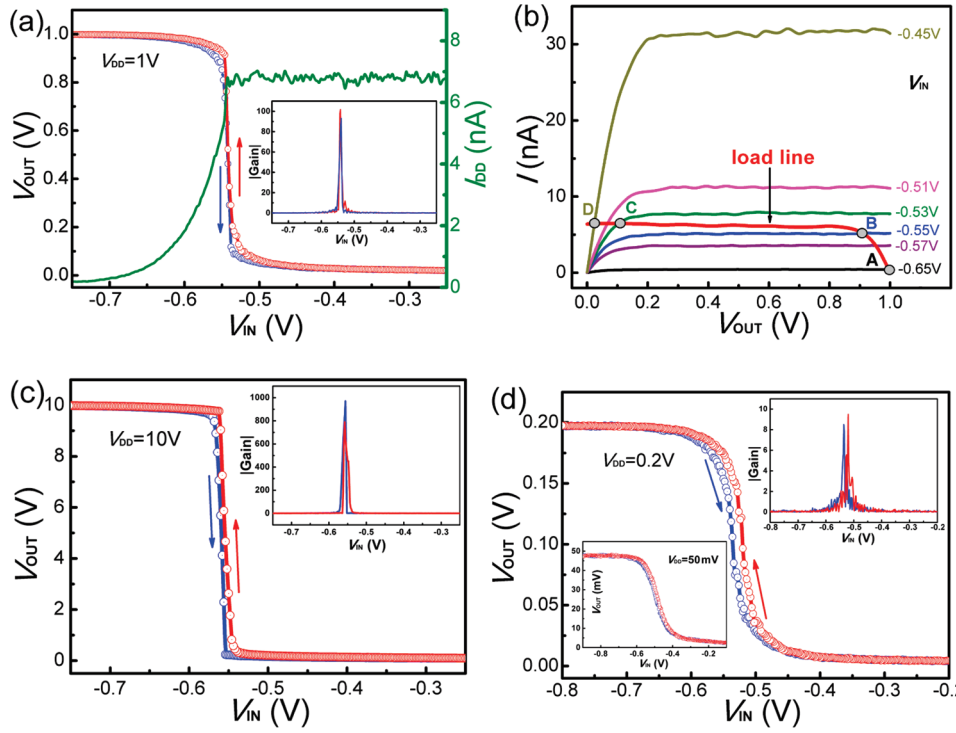


**Figure 3. (a) Static VTC curves of the NMOS inverter under the $V_{DD}$ of 1 V with $V_{IN}$ being cycled. The arrows indicate the $V_{IN}$ sweeping directions. The green curve shows the current flowing through the inverter ($I_{DD}$) during the measurement (corresponding to the red VTC curve). The inset is the voltage gain curves obtained from the corresponding VTC curves. (b) Graphical determination of the static VTC of the inverter. A, B, C, and D are corresponding operating points at four representative $V_{IN}$. (c) VTC curves of the inverter under $V_{DD}$ of 10 V. The inset is the corresponding voltage gain curves. (d) VTC curves of the inverter under $V_{DD}$ of 0.2 V. The upper-right inset shows the corresponding voltage gain curves. The lower-left inset shows the VTC curves under an ultra low $V_{DD}$ of 50 mV.**

inverter constructed with the above-mentioned two transistors with the input voltage ($V_{IN}$) being cycled ($V_{DD}$ = 1 V). The arrows indicate the $V_{IN}$ sweeping directions. The high and low output voltages ($V_{OH}$ and $V_{OL}$) are close to the supply voltage $V_{DD}$ and zero, respectively. The green curve shows the current flowing through the inverter ($I_{DD}$) during the measurement (corresponding to the red VTC curve). It is clear that the $I_{DD}$ is less than 7 nA during the whole measurement process, corresponding to a power consumption <7 nW, which is so far the lowest reported value for NMOS and/or PMOS inverters. The inset shows the voltage gain ($= -dV_{OUT}/dV_{IN}$) curves obtained from the corresponding VTC curves. The peak gain value is as high as ~100, which is the best reported value, as far as we know, for inverters based on nanomaterials working at a supply voltage of 1 V.

To explain why the NMOS inverter exhibits such high performance, we have studied the operation of the inverters in detail. Figure 3b illustrates the graphical determination of the static VTC of the inverter (all the curves are the experimental results, $V_{DD}$ = 1 V). In our inverter, the gate and source of the load transistor are connected, hence the gate voltage of the load can always be taken as 0 V (*i.e.*, $V_{GS\text{-}L}$ = 0 V). Therefore, the $I_{DS\text{-}L}-V_{DS\text{-}L}$ relation (*i.e.*, $I_{DS}-V_{DS}$ relations of load transistor) at $V_{GS\text{-}L}$ = 0 V is the load line of the inverter. The marked A, B, C, and D are four representative intersections of the load line and the $I_{DS\text{-}D}-V_{DS\text{-}D}$ curves ($I_{DS}-V_{DS}$ relations of driver transistor) at various $V_{IN}$ ($= V_{GS\text{-}D}$), which reflect the actual operating points of the inverter. Since the load has a near-0 $V_{th}$, its saturation current at $V_{GS\text{-}L}$ = 0 V is very small (see Figure 2a,b), which directly results in low power consumption of this inverter. At operating point A, $V_{IN}$ is −0.65 V (input logic 0), and the driver is cut off, resulting in a very small $I_{DD}$ (see Figure 2c,d). Therefore, $V_{OUT}$ is very close to $V_{DD}$ ($V_{OUT} = V_{DD}-V_{DS\text{-}L}$) (output logic 1). With $V_{IN}$ increasing, $V_{OUT}$ decreases. When $V_{IN}$ changes from −0.55 to −0.53 V (corresponding to points B and C), $V_{OUT}$ decreases sharply from 0.9 to 0.1 V, corresponding to an ultrahigh voltage gain. When $V_{IN}$ increases further to −0.45 V, the operating point reaches point D (input logic 1), and $V_{OUT}$ is very close to zero (output logic 0). From this figure we can see that in our case, the perfect $I_{DS}-V_{DS}$ saturation characteristics of both the load and driver transistors account for the ultrahigh voltage gain of the inverter, while the small saturation current for the load at $V_{GS\text{-}L}$ = 0 V (corresponding to a near-0 $V_{th}$ for the load) accounts for the low power consumption and the near-ideal $V_{OH}$ and $V_{OL}$ values.

Figure 3c shows the VTC curves of the inverter at $V_{DD}$ =10 V. Maximum voltage gain can be as high as ~1000 (see the inset) with very stable output voltage. Figure 3d shows the VTC curves of the inverter under $V_{DD}$ = 0.2 V. The peak gain is about 10 (see the upper-

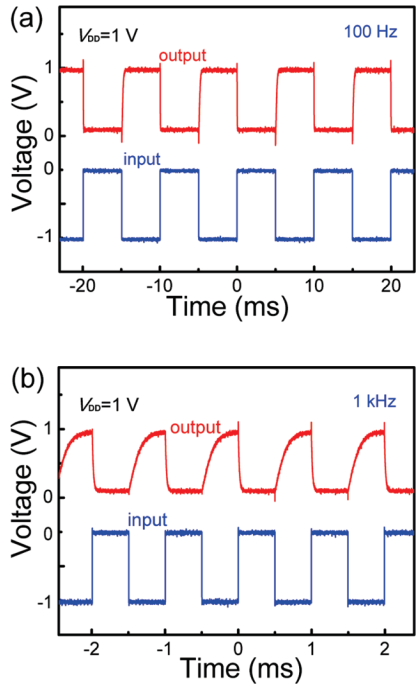


**Figure 4. Dynamic behaviors (red curves) of the NMOS inverter driven by square wave with frequencies of 100 Hz (a) and 1 kHz (b) at $V_{DD}$ of 1 V. The blue curves show the corresponding square wave inputs.**

right inset). The lower-left inset shows the VTC curves of the inverter under $V_{DD}$ = 50 mV. It can be clearly seen that the inverter still exhibits good inverting behavior under this ultra low supply voltage. As far as we know, this is the lowest reported supply voltage under which an inverter based on nanomaterials can still work with good inverting behaviors at room temperature. This low voltage behavior is valuable for low power consumption application.

We have also measured the dynamic behavior of the inverter driven by square wave with different frequencies at $V_{DD}$ of 1 V. The high and low levels of the input square wave are 0 and −1 V, respectively. At a lower frequency of 100 Hz (Figure 4a), good inverting behaviors are clearly observed. At a higher frequency of 1 kHz (Figure 4b), RC delays at on and off switching are observed. The rising ($t_r$) and falling times ($t_f$) can be obtained to be about 0.25 and 0.03 ms, respectively, measured at 10% and 90% output values from Figure 4b. The delays mainly result from the overlap capacitance between the $V_{IN}$ and $V_{OUT}$ electrodes in our inverter structure.[23−26] The difference of $t_r$ and $t_f$ ($t_r/t_f \cong 8$) could be understood by considering the difference between the on-state current levels of load (~0.35 μA) and driver transistors (~2.7 μA) (see Figure 2b,d). Channel electrons charge and discharge the overlap capacitance region with the channel current of the driver being about 8 times larger than that of the load, resulting in $t_r$ being about 8 times larger than $t_f$. The inverter can be further improved in the future to minimize the delays by using active semiconductor materials of higher carrier mobility and thinner gate dielectrics, shortening the channel length, and optimizing the measurement system.[6] Finally, it is worth noting that the performance of the inverters remain stable after they have been exposed to air continuously for 3 or more months.

## CONCLUSION

In summary, we have fabricated ultrahigh-performance inverters, each consisting of two top-gate Au/$HfO_2$/CdS NB MOSFETs. The inverters show many characteristics, such as large $V_{DD}$ range (from 50 mV to 10 V), ultrahigh voltage gain, and low power consumption. The $V_{OH}$ and $V_{OL}$ are very close to full rail. The inverters also show good dynamic behavior with square wave input frequencies of up to 1 kHz. The performance of the inverters is stable with time. The operation of the inverters is analyzed in detail. These inverters are promising for future low power high performance logic circuit applications.

## EXPERIMENTS

The *n*-CdS NBs used for fabricating devices were synthesized *via* an atmospheric vapor−liquid−solid (VLS) method.[18] During the synthesis process, CdS powders (99.995%) were placed at the upstream of Ar gas as the source. Si wafers covered with 10 nm thick thermally evaporated Au films were used as substrates. A tiny Cd grain (99.95%) was placed between the source and the substrates as the dopant. The temperatures at the source and substrate locations were about 850 and 750 °C, respectively. The dopant temperature could be changed from 750 to 850 °C by changing the position of Cd grain. By controlling the mass ratio of CdS to Cd and the position of Cd grain, we could partially control the electron concentration of the CdS NBs. The as-synthesized CdS NBs exhibited good *n*-type conductivity due to sulfur vacancies and/or cadmium interstitials, which serve as shallow donors.

The MOSFETs employed in the inverters were fabricated as follows: First, CdS NB suspension was dropped on oxidized Si substrates, each covered with a 400 nm thick $SiO_2$ film. Second, UV lithography followed by thermal evaporation and lift-off process was used to fabricate ohmic contact In/Au electrodes (20/100 nm) on individual *n*-CdS NBs. The spatial distance between the ohmic electrodes on each NB was about 20 μm. Third, a high-κ dielectrics $HfO_2$ film (20 nm) was deposited to clad the NB by atomic layer deposition (ALD) method. Finally, an Au top-gate electrode (~3 μm wide, 100 nm thick) was made across the $HfO_2$/NB in between the In/Au electrodes by a similar process as mentioned above. Here, two kinds of CdS NBs, labeled as NBs A and NBs B, were employed to fabricate the two types of MOSFETs used in the inverter. The electron concentrations of NBs A were around $1 \times 10^{16}$ $cm^{-3}$, while those of NBs B were around $5 \times 10^{16}$ $cm^{-3}$. The electron concentrations of the CdS NBs can be obtained by measuring CdS NB back-gate FETs before depositing the $HfO_2$ layer.[18] To construct high-performance inverters, the MOSFETs based on CdS NBs A were used as the loads, while those based on CdS NBs B were used as the drivers.

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